REMARKS

Claims 1-35 are pending.

In the Office Action Summary, the Examiner indicates that only Claim 1 is pending. Applicants respectfully submit that Claims 1-35 are pending.

In the Preliminary Amendment filed on April 14, 2004, Claim 1 was amended. However, there was no instruction or statement that Claims 2-35 are canceled. Should the Examiner disagree, Applicants request clarification as to the basis for the Examiner's cancellation of Claims 2-35.

As set forth in 37 CFR §1.173(b)(2):

> *Claims.* An amendment paper must include the entire text of each claim being changed by such amendment paper and of each claim being added by such amendment paper. For any claim changed by the amendment paper, a parenthetical expression "amended," "twice amended," *etc.*, should follow the claim number. Each changed patent claim and each added claim must include markings pursuant to paragraph (d) of this section, **except that a patent claim or added claim should be canceled by a statement canceling the claim** without presentation of the text of the claim. (Emphasis added.)

As there was no statement to cancel Claims 2-35, Claims 2-35 are pending in the application. If for some reason the Examiner believes Claims 2-35 were canceled, Applicants hereby request reinstatement and examination of Claims 2-35.

The obviousness-type double patenting rejection is traversed.

The Examiner states:

> Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,395,578. (Office Action, page 2.)

This rejection is respectfully traversed. Applicants note that the present Application is a reissue of U.S. Patent No.

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

6,395,578. Applicants request that the Examiner recite the basis for the Examiner's assertion that a Terminal Disclaimer is required for a reissue application based on the patent being reissued.

Applicants note that the terminal part of the term of a patent is not disclaimed if the prior patent is reissued. Specifically, Applicants refers the Examiner to PTO form PTO/SB/26, entitled "TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A PRIOR PATENT", which recites:

> In making the above disclaimer, the owner **does not disclaim the terminal part of the term of any patent granted on the instant application** that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," **in the event that said prior patent later:**
> ...
> **is reissued**; or
> is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Accordingly, Applicants submit that the Terminal Disclaimer is effectively obviated upon reissuance of the prior patent.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claim 1 is patentable over Kinsman (6,172,419) in view of Ohsawa et al. (6,093,970).

With regards to Kinsman, the Examiner admits:

> Kinsman teaches the above outlined features **except for singulating the circuit board strip into semiconductor packages**. (Office Action, page 3, emphasis added.)

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
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Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

To cure this glaring deficiency in Kinsman, the Examiner further asserts:

> However, Ohsawa discloses a semiconductor device with (1) … singulating the circuit board strip into semiconductor packages (see Figure 2G). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Klnsman (accordance with the teaching of Ohsawa). Doing so would facilitate the manufacture of the semiconductor and reduce the operational cost. (Office Action, page 3.)

The Examiner's statement is respectfully traversed. Applicants respectfully submit that one of skill in the art would have no motivation to combine Kinsman with Ohsawa et al. as asserted by the Examiner.

Applicants note that Kinsman teaches:

> Substrate 102 can be of either a single or multi-layered construction as is commonly known in the art, and typically is formed from an **organic epoxy-glass resin based material, such as bismaleimide-triazin (BT) resin or FR-4 board** as is commonly known in the art. (Col. 4, lines 30-34, emphasis added.)

In stark contrast, Ohsawa et al. teaches:

> FIGS. 2(A) to (I) are cross-sectional views showing the process steps for making **a film circuit** and **making a reinforcing plate adhere to the back surface of the film circuit** in accordance with the present invention.. (Col. 4, lines 62-65.)

Applicants respectfully submit that one of skill in the art would have no motivation to modify the resin based substrate process of Kinsman with the film circuit process of Ohsawa et al. as suggested by the Examiner as a resin based substrate is substantially different than a film circuit as those of skill in the art understand.

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

As set forth in the MPEP 2143.01, at page 2100-131, Rev. 2, May 2004:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (Emphasis in original.)

Further, Applicants respectfully submit that the Examiner is using improper hindsight reconstruction to deprecate the Applicants' claimed invention.

For at least the above reasons, Kinsman in view of Ohsawa et al. does not teach or suggest:

> A method for fabricating semiconductor packages, the method comprising:
> **providing a circuit board strip including a plurality of unit circuit boards**, each unit circuit board having a plurality of first ball lands formed at a first major surface thereof, a plurality of bond fingers formed at an opposite second major surface thereof, vias through the circuit board each electrically connected between a bond finger and a first ball land, and a through hole between the first and second major surfaces;
> **receiving in each through hole a semiconductor chip** having a first major surface, and an opposite second major surface provided with a plurality of input/output pads thereon, wherein the second major surface of the chip faces in the same direction as the second major surface of the respective circuit board;
> electrically connecting the input/output pads of each semiconductor chip with associated ones of the bond fingers of the respective circuit board;
> **encapsulating the semiconductor chips, and filling the through hole of each unit circuit board of the circuit board strip using an encapsulating material**;
> fusing conductive balls on the first ball lands of each unit circuit board;
> **singulating the circuit board strip into semiconductor packages respectively corresponding to the unit circuit boards**,

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

as recited in Claim 1, emphasis added. Accordingly, Claim 1 is allowable. Claims 2-35, which depend from Claim 1, are allowable for at least the same reasons as Claim 1.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

Claims 1-35 are pending in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 25, 2005.

Attorney for Applicant(s) — April 25, 2005 Date of Signature

Respectfully submitted,

Serge J. Hodgson
Attorney for Applicant(s)
Reg. No. 40,017
Tel.: (831) 655-0880

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888